Application Report
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Amplifiers and Bits: An Introduction to Selecting Amplifiers for Data Converters

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ABSTRACT

This application report discusses various considerations that must be taken into account when interfacing general-purpose amplifiers and analog-to-digital converters. The report discusses bandwidth, resolution, analog ADC input drive, and power supply considerations for both parts.

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1 Introduction

This application report discusses various considerations that must be taken into account when interfacing operational amplifiers and analog-to-digital converters (ADC). Although much of the discussion is related to low speed applications, material is also presented that relates to high-speed interfaces. Appendix A discusses some of the criteria necessary to define the interface between an operational amplifier and an analog to digital converter in one type of application that has extremely critical performance constraints—a cellular telephone base station. Figure 1 shows the amplifier-ADC interface:

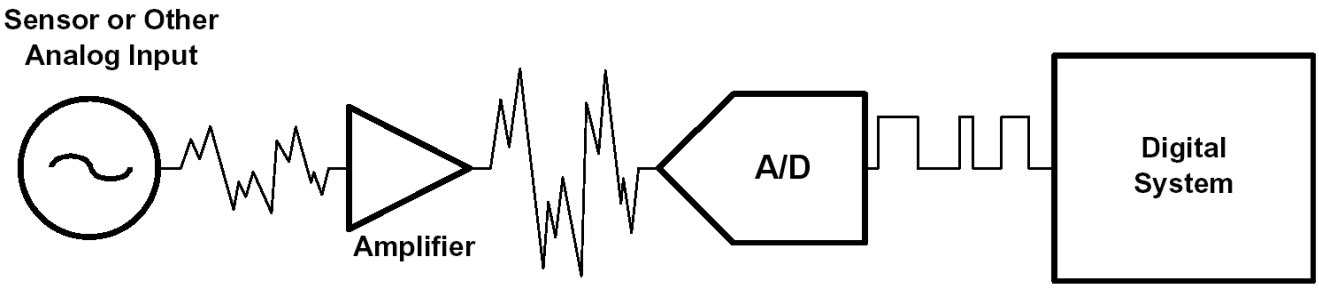

Figure 1. Amplifier and ADC

The process of interfacing an input to an analog to digital converter may involve some or all of the following processes:

- Amplification / attenuation – scaling the input signal level to the level required by the input circuitry of the ADC.
- DC offsetting / level shifting – moving the dc level of the input signal up or down by a fixed offset to match the operating range of the ADC.
- Filtering – removing unwanted signal components from the input signal, and providing only the bandwidth of interest to the ADC.

Fortunately, op amps are well suited to all of these functions. Often times, a single op amp can be made to perform multiple functions. Each application is, in a sense, a special case. It is the designer's responsibility to understand the characteristics of the data converter, input signal, power supply, and other system requirements prior to determining the op amp interface that presents the input source to the ADC. For example, a temperature sensor outputs a direct current or voltage, and dc characteristics of the signal are vital. An RF application, on the other hand, can be ac coupled and therefore dc characteristics of the op amp can be discounted.

2 The Importance of Buffering

One of the advantages of the op amp interface to the ADC that is often overlooked is buffering. Most ADCs do not have an input voltage range that exactly matches the range presented by the source. There are rare cases when the voltage source output matches the ADC. The temptation in these cases would be to delete the op amp interface. However, the designer may still want to consider a buffer op amp between the input signal and the converter. There are many reasons for this, but the most common include:

- Impedance matching: Signal sources are not necessarily low impedance. The input of an ADC may well load the source, affecting it. A unity-gain op amp buffer has very high input impedance, and therefore will not load the source. In addition, its low output impedance is well-suited to driving the input of an ADC.
- Reducing the effects of capacitive loading: Most types of ADCs present a capacitive as well as resistive load on their input. This requires an external compensation circuit, usually a resistor and capacitor. Texas Instruments often specifies this network. It is important to follow the recommendation, but doing so presents a capacitive load to the source. The

resistor isolates the source from the capacitor, but is usually a low value. The low output impedance of an op amp interface can usually drive this network with no problem.

- Conversion from single-ended to differential signals: Even if an op amp is not required for the reasons above, many new analog to digital converters have differential inputs. Most input sources are single ended. Therefore, an op amp interface is required to perform the conversion. This conversion can be accomplished with single-ended op amps, but is more readily accomplished by use of a fully differential op amp.

3 Bandwidth

Choosing an ADC that meets the system requirements for bandwidth is the first priority. Other considerations such as power or interface also come into play, but once the bandwidth of the ADC has been determined, an amplifier can be chosen to go with it. Applications observe Nyquist and sample at greater than twice the highest frequency of interest to avoid aliasing. If the Nyquist limit were the only important factor, then this discussion could stop here. Unfortunately, the question of *how much bandwidth is enough?* is far more complicated.

Any discussion of op amp bandwidth begins with the Bode plot of open loop response. This plot is available in the data sheet of any op amp, and looks something like the plot in Figure 2.

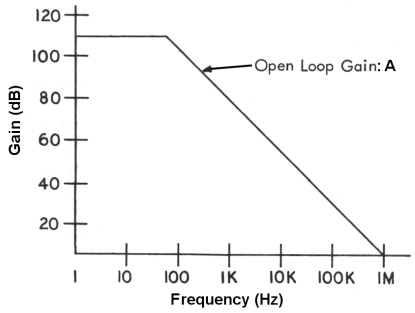

Figure 2. Open Loop Bode Plot of an Op Amp

A Bode plot is a plot of frequency versus gain for an op amp. Both axes are logarithmic, with the gain being plotted in decibels (dB). Knowing only a few points on its Bode plot can approximate the performance of any compensated voltage feedback op amp:

- The open loop gain (A) at DC and low frequencies, which is characterized by a horizontal line (gain is constant with frequency).
- The breakpoint due to the internal compensation. At this point, the op amp response changes from being constant with frequency to a region with a rolloff of 20 dB per decade of frequency.
- The point at which the rolloff of the frequency reaches the unity gain (0 dB) line on the Bode plot. This is considered the bandwidth of the amplifier.

The Bode plot defines the legal operating point of the op amp, the same as characteristic curves define the operating point of a transistor. An op amp can be operated anywhere to the left and underneath the curve of the open loop gain. Operating an op amp in a region near the curve, however, can have unexpected results. These results are quite different for the inverting and noninverting gain configurations, and are discussed in more detail below.

3.1 Feedback Theory

Op amps are operated with feedback—in a closed loop configuration. The general formula for feedback systems can therefore be applied to op amps:

$$\frac{V_O}{V_I} = \frac{A}{1 + A\beta} \tag{1}$$

This expression defines some important terms:

- The quantity A, which is known as the open loop gain
- The quantity Aβ, which is known as the loop gain

These are shown graphically in Figure 3:

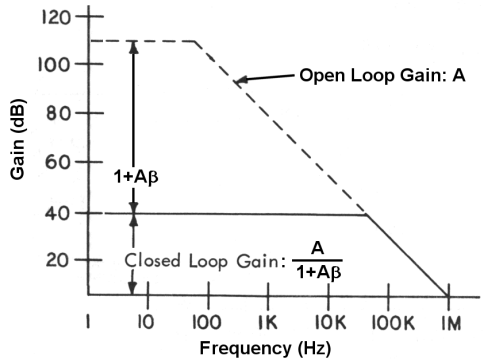

Figure 3. Closed Loop Bode Plot

The closed loop gain modifies the open loop gain A by 1+Aβ. Because logarithms are being used, divisions can be accomplished by subtraction of the quantities. Therefore, at low frequencies before the internal compensation break point, the closed loop gain in the figure above is 110 dB – 70 dB, or 40 dB.

The sacrifice in gain is accompanied by an increase in bandwidth. Instead of the constant (horizontal) gain line intersecting breaking at the internal compensation frequency (about 100 Hz in figures 2 and 3); it intersects at about 50 kHz. This decrease in gain and increase in bandwidth is a linear function known as the *gain bandwidth product*, or GBP.

With VFB amplifiers, GBP is the specification of interest when looking at small signal bandwidth. Because the VFB amplifier is dependent on the gain that is being employed, the frequency of the signal of interest multiplied by the gain must be less than the GBP for the amplifier.

3.2 Closed Loop Bandwidth

It should be noted at this point that for both noninverting and inverting amplifier stages, the actual gain is a function of both the closed and open loop gains. Designers may not be familiar with this fact, because in most cases the contribution from the open loop gain is negligible. The implications of this fact are discussed in the sections below.

3.2.1 Noninverting Closed Loop Bandwidth

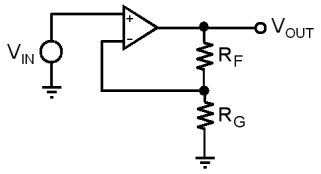

Figure 4. Noninverting Gain Stage

For noninverting op amp gain stages, the exact gain can be calculated by:

$$\frac{V_O}{V_I} = \frac{A}{1 + \frac{A \cdot R_G}{R_G + R_F}} \quad \text{If A >> desired closed loop gain, } \frac{V_O}{V_I} = 1 + \frac{R_F}{R_G} \qquad (2)$$

Where:

R_G is the gain resistor of the stage

R_F is the feedback resistor of the stage

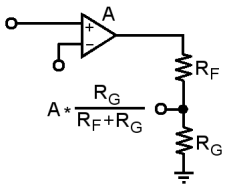

Figure 5. Noninverting Stage With Loop Broken

The quantity $\frac{R_G}{R_G + R_F}$ is the proportion of output voltage fed back the input (from the voltage divider rule).

Equation (2) defines the noninverting closed loop gain. The point at which the closed loop gain intersects the open loop gain curve of the op amp is the closed loop bandwidth. Therefore, the gain bandwidth product (GBP) is equal to:

GBP = (noninverting closed loop gain) x (closed loop bandwidth) (4)

Designers are probably much more familiar with the expression $\frac{V_O}{V_I} = 1 + \frac{R_F}{R_G}$, but should keep in mind it is an approximation based on infinite open loop gain.

3.2.2 Inverting Closed Loop Bandwidth

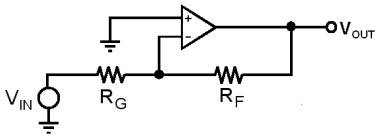

Figure 6. Inverting Gain Stage

The gain bandwidth product derived above only truly applies to noninverting gain stages. For inverting op amp gain stages, the exact gain can be calculated by:

$$\frac{V_O}{V_I} = \frac{\frac{-A \cdot R_F}{R_G + R_F}}{1 + \frac{A \cdot R_G}{R_G + R_F}} \quad \text{If A >> desired closed loop gain, } \frac{V_O}{V_I} = -\frac{R_F}{R_G} \qquad (5)$$

Designers are probably much more familiar with the second expression. Comparing this equation to the general form of the feedback equation (1), the open loop gain of the inverting gain stage is equal to:

$$\frac{-A \cdot R_F}{R_G + R_F} \qquad (6)$$

This has implications for the gain bandwidth product of the inverting gain stage. When the inverting configuration is used, the open loop gain is affected by the feedback and gain resistors R_F and R_G. Figure 7 shows the effect on bandwidth:

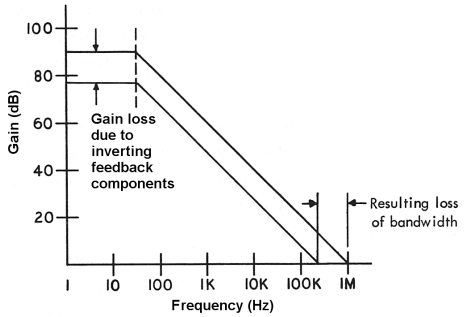

Figure 7. Effect of Inverting Stage Components on Gain

For the unity gain stage, where $R_G = R_F$, the gain is reduced by 1/2.

This effect can be calculated visually on the open loop Bode plot. Simply draw a horizontal line corresponding to the reduced gain to the compensation break point frequency, then draw a diagonal line parallel to the original open loop plot down to the 0 dB axis. This is the adjusted gain plot for the op amp stage with inverting gain resistors.

Another way of expressing this is that for an inverting amplifier of gain one, half of the output signal is fed back, similar to a noninverting gain of 2.

Therefore, high-speed applications, where the speed of the interface is the dominant requirement, should use the noninverting configuration. If common mode rejection, noise, and harmonic distortion are the dominant requirements, then the inverting configuration should be used.

3.3 Gain Bandwidth Safety Margin

It is good design practice to ensure the GBP of the amplifier has some amount of extra margin. 40 dB is a good safety margin, which insures that the error due to the open loop characteristics of the op amp is minimized.

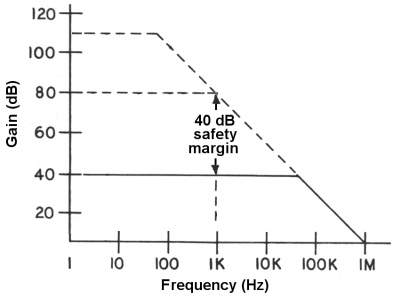

Figure 8. Safety Margin Limiting Bandwidth

For the Bode plot of the *1 MHz* op amp shown in Figure 8, if a gain of 40 dB (X100) is desired, this means that the maximum usable frequency is only 1 kHz. This is one reason why a high-speed op amp may be required, even for relatively low-speed systems.

The reason for this 40 dB safety margin is that for both the inverting and noninverting gain configurations, there is a dependence on open loop gain (A) in the closed loop gain calculation (see equations 2 and 5). For a 40 dB difference between closed and open loop gain, inverting and noninverting gain errors are of the order of 0.01%. If the safety margin is decreased to 20 dB, gain error are of the order of 2%. These are substantial gain errors and should be avoided.

If more accuracy is needed, the safety margin should be increased. Utilizing op amps with high gain bandwidth products at lower gains can do this. If accuracy is a more important consideration than noise, more than one op amp operated at a lower gain is better than a single op amp operated at high gain. Accuracy increases dramatically as the safety margin is increased. For a safety margin of 60 dB, the gain errors are in the order of 0.0001%. Table 1 shows the effect of safety margin on gain accuracy for inverting and noninverting stages.

Safety Margin (dB)	Inverting Gain Error (%)	Non-inverting Gain Error (%)
0	66.6	50
10	16.7	9.09
20	1.96	0.99
30	0.2	0.0999
40	0.02	0.01
50	0.002	0.001
60	0.0002	0.0001
70	0.00002	0.00001
80	0.000002	0.000001

Table 1. Safety Margin vs Gain Error

These figures come from equations (2) and (5). For a given safety margin, a noninverting stage has lower gain error.

There is an additional problem associated with the open loop dependence. Referring to Figure 8, there is a slight frequency dependence associated with the closed loop gain. The safety factor at 1 kHz is 40 dB, at 100 Hz the safety margin has increased to 60 dB. Therefore, there is a slight change in gain.

Most designers are unaware of the open loop effects on op amp gain circuits because they are used to designing with low gains, utilizing op amps with high gain bandwidth products. The error produced by the open loop gain of the op amp is much less than the accuracy of the resistors used to define the closed loop gain. It is somewhat analogous to the case of special relativity. The really bizarre effects of special relativity do not show up until one is traveling very close to the speed of light. The really bizarre effects of open loop gain on closed loop gain do not show up until one is operating with a low safety margin.

3.4 Gain Bandwidth Dependence on Supply Voltage

The supply voltage used with an op amp can also affect the GBP. As an example, Figure 9 shows that the TLV2460 has a delta of 400 kHz of GBP across the full V_{DD} range for the device.

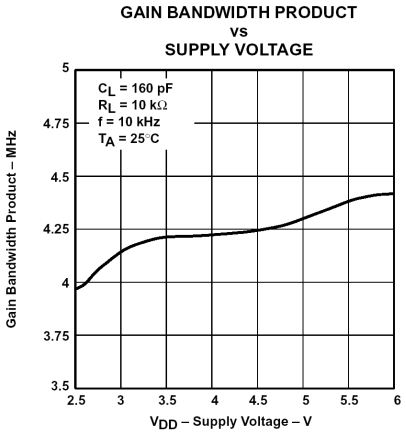

Figure 9. Typical Gain Bandwidth Product Graph (TLV2460)

4 Slew Rate

Another specification that is of interest with respect to large signal bandwidth is slew rate (SR). Slew rate becomes important when signal levels are large (close to the voltage rails of the op amp), or signals have a non-sinusoidal nature (square waves, pulses, triangle waves, sawtooth waves, ramps, etc.) These waveforms have harmonic content that may exceed the bandwidth of the op amp.

The slew rate is defined as the rate of change in the output voltage caused by a step change at the input. It is expressed in V/μs or V/ns. The slew rate specified for an op amp is the maximum SR it will pass and is generally specified with a gain of 1. The following figure shows SR graphically.

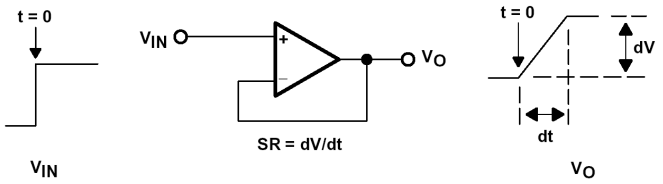

Figure 10. Slew Rate

In order for an amplifier to pass a signal without distortion due to insufficient SR, the amplifier must have at least the maximum SR of the signal. The maximum SR of a sine wave occurs as it crosses zero. The following equation defines this slew rate:

$$SR = 2\pi fV \quad (7)$$

Where:

f = frequency of the signal
V = peak voltage of the signal

The SR is sometimes represented as SR+ and SR-. SR+ is the abbreviation for the slew rate for a positive transition and SR- is the abbreviation for the slew rate for a negative transition. Many applications are best served when SR+ and SR- are the same magnitude.

The primary factor controlling SR in most op amps is an internal compensation capacitor that is added to make the op amp unity gain stable. Remember however, that not all op amps have compensation capacitors. In op amps without internal compensation capacitors, the SR is determined by internal op amp parasitic capacitances. Noncompensated op amps generally exhibit faster SR than decompensated op amps and decompensated op amps exhibit faster slew rate than fully compensated op amps. When noncompensated or decompensated op amps are used the designer must ensure the stability of the circuit by external components.

5 Noise and Bits

As might be expected, noise degrades the performance of the buffer op amp A/C converter combination. This section describes the degradation.

Op amp data sheets have different ways of expressing the noise. Unfortunately, these noise specifications overlap in some cases.

- The first way is to specify noise as a function of the bandwidth, both giving a constant value for the white noise characteristic in nV or $\mu V / \sqrt{Hz}$.
- The second way is to specify noise graphically. The specification above only applies to the constant *white noise* portion of the graph. The specification is not valid at low frequencies - *pink noise* portion of the graph where the noise rapidly increases, proportional to the inverse of frequency (1/f). Figure 11 is an example of the noise graph for an op amp.

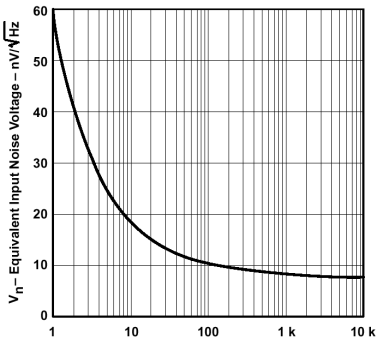

Figure 11. Noise Characteristic of a Typical Op Amp

- The last way is to combine it as a Total Harmonic Distortion + Noise Specification

The designer is left with the responsibility of determining the best method of specifying noise. Generally, if the bandwidth is broad, the first method may be the best. Even if there is not a separate THD specification, noise probably predominates the THD + Noise expression. If the bandwidth is narrow, the contribution from noise is probably much less, and the THD + N specification can probably be used.

5.1 Noise From the Graph

The designer should try to select an op amp that does not have a 1/f noise characteristic that overlaps the bandwidth of interest.

In Figure 8, the noise is relatively constant with frequency down to 100 Hz. Below 100 Hz, the noise increases exponentially. If noise is a consideration, this op amp should not be used at a frequency below 100 Hz. Many applications are ac-coupled, and an op amp can be selected with a noise breakpoint below the frequency range of interest.

5.2 Noise From the nV or $\mu V / \sqrt{Hz}$ Specification

The noise specification for an op amp is found in its data sheet. This number is usually given in $nV / \sqrt{Hz}$.

Once an op amp has been selected with the 1/f noise portion below the bandwidth of interest, the total noise can be calculated from the noise specification. The designer needs to know the bandwidth of the system. That is, the highest frequency that is passed through the op amp minus the lowest frequency that is passed through the op amp. Assume an op amp with a low frequency noise breakpoint of 10 Hz, a noise specification of $8\text{nV}/\sqrt{\text{Hz}}$, and that it is used in a frequency range of 20 Hz to 20 kHz:

- To begin with, the 10 Hz noise breakpoint is below the lowest frequency of interest, therefore the constant noise specification of $8\text{nV}/\sqrt{\text{Hz}}$ can be assumed for all frequencies within the bandwidth.
- Next, calculate the *root Hz* part: $\sqrt{20000-20}=141.35$
- Multiplying this by the noise spec: $8\times141.35=1.131\mu\text{V}$

This is the *equivalent input noise* or EIN. The output noise equals the input noise multiplied by the gain. The output noise, of course, is what is coupled to the ADC converter.

The op amp noise may not be the only source of noise in the system. Other noise sources may include noise from previous stages of filtering, offset, or signal conditioning, etc. Noise sources add according to the root sum square law:

$$E_{rms}=\sqrt{e_{1rms}^2+e_{2rms}^2+...e_{nrms}^2} \qquad (8)$$

Once the contribution from all potential noise sources has been taken into account, then it can be used in subsequent calculations.

5.3 Total Harmonic Distortion Plus Noise

The total harmonic distortion plus noise op amp parameter, THD+N, is defined as the ratio of the RMS noise voltage plus the RMS harmonic voltage of the fundamental signal to the fundamental RMS voltage signal at the output. It is expressed in dBc or %.

dBc is a common usage, and is a relative term with a variable reference, like dB alone. It means *dB referenced to a carrier level*. For example, *Spurious signals less than -50 dBc* means that spurious signals will be at least 50 dB less than some specified carrier level present (which also means *50 dB less than the desired signal*).

THD + N compares the frequency content of the output signal to the frequency content of the input. Ideally, if the input signal is a pure sine wave, the output signal is a pure sine wave. Due to nonlinearity and noise sources within the op amp, the output is never pure.

To state another way, THD + N is the ratio of all other frequency components to the fundamental.

$$\text{THD}+\text{N}=\left[\frac{\left(\sum\ \text{Harmonic Voltages}+\text{Noise Voltages}\right)}{\text{Fundamental}}\right]\times100\% \qquad (9)$$

Typically an op amp must be operated at or below its recommended operating conditions to realize low THD.

Unfortunately, if the THD is coupled with the noise in this way, the designer may have no choice but to add the noise calculated from the nV or $\mu V / \sqrt{Hz}$ specification to the THD+N specification. Fortunately, these two specifications are uncorrelated, and are therefore added according to the root sum squared method:

$$E_{rms} = \sqrt{e_{1rms}^2 + e_{2rms}^2 + ...e_{nrms}^2} \quad (10)$$

5.4 Signal to Noise Ratio

The title of this section is descriptive of this specification. It can be approached from the op amp side of the interface as well as the ADC converter side, and the performance of the two matched. In practice, the op amp signal to noise ratio should be much better than that of the ADC converter, to avoid limiting its performance.

Assuming that the noise level is now known, the signal level divided by the noise level, gives the signal to noise ratio. If both are expressed in dB, the noise level can simply be subtracted from the signal level.

The ADC signal to noise ratio can also be determined in terms of the bits of the converter:

$$SNR\ dB = 6.02 \times n - 1.76 \quad (11)$$

or

$$n = \frac{SNR\,dB + 1.76}{6.02} \quad (12)$$

Equation 12 is a quick approximation of the number of converter bits required for the application. It is valid for sinusoidal signal signals only, and assumes 0 INL and 0 DNL error in the converter. A simple table can be constructed for the number of data converter bits versus SNR:

Number of Bits (n)	SNR (dB)
4	22.32
8	46.4
10	58.44
12	70.48
14	82.52
16	94.56
18	106.6
20	118.64
22	130.68
24	142.72

Table 2. Signal to Noise Ratio vs Converter Bits

5.5 SINAD

Once the Total Harmonic Distortion + Noise (THD + N) specification is known, it can be used to calculate the SINAD. A brief introduction to the SINAD is in order.

SINAD is a figure of merit used to describe the quality of the signal. It is basically a measure of the distortion present in an audio signal due to noise and harmonics. The general form for mathematical expression of SINAD is as follows:

$$\text{SINAD} = \frac{\sum(\text{All Frequency Components})}{\sum(\text{All Frequency Components} - \text{Fundamental Component})} \tag{13}$$

The SINAD ratio of the modulated signal is computed by removing the fundamental signal and then by expressing the RMS value of the remaining power spectrum in decibels relative to the RMS value of this same power spectrum in which the fundamental signal has been removed. The ratio of the composite signal to the noise plus distortion component is the SINAD ratio.

SINAD can also be defined as:

$$\text{SINAD} = \text{SNR} + \text{D} = \frac{\text{Signal} + \text{THD} + \text{N}}{\text{THD} + \text{N}} \tag{14}$$

Hence the name SINAD (**SI**gnal to **N**oise **A**nd **D**istortion)

NOTE: These numbers are scalar and not in dB.

To summarize – SNR is the ratio of energy in the fundamental signal and the energy in noise. Total harmonic distortion (THD) is a similar ratio between the energy in the harmonics and the energy in the fundamental.

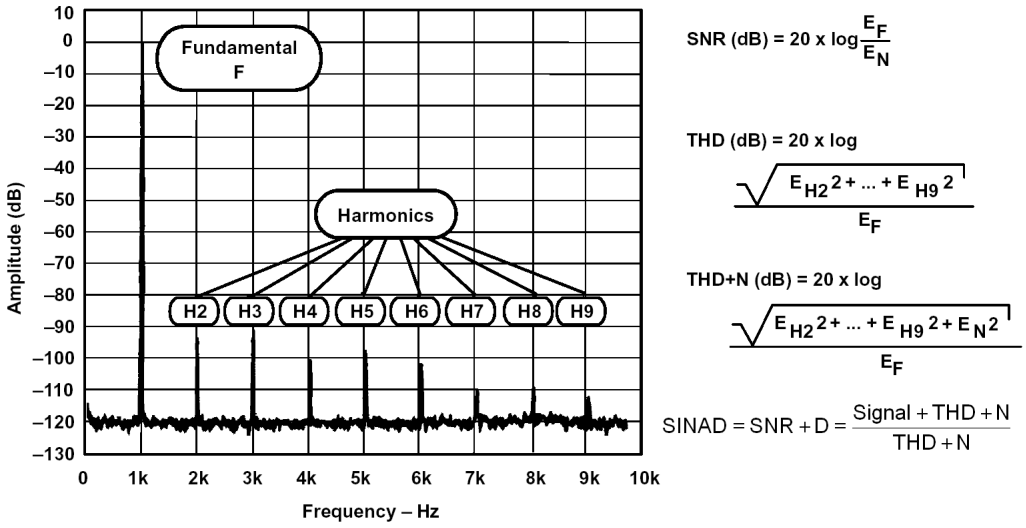

Figure 12. SNR and THD Pictorial

5.6 Effective Number of Bits (ENOB)

A given converter is advertised as having a certain number of bits, the common sizes being given in Table 2 above. The converter itself has limitations that degrade its own performance. These are discussed in the next section. The SNR and THD of the buffer op amp degrade the performance of the ADC conversion system, lowering the number of meaningful (effective) bits of information that it can provide to the data processing elements of the system.

SINAD takes into account the harmonics and the noise energy, and thus produces a real SNR that can lead to the effective number of bits. ENOB is defined as:

$$\text{ENOB} = \frac{[(\text{SINAD dB}) - 1.76]}{6.02} \tag{15}$$

Data converter specifications offer either SNR + D or THD + N in dB; thus, this equation is easy to use. Conversely, amplifier specifications usually specify SNR + D or THD + N in percent instead of dB. This requires some mathematical manipulation to use the same equations.

Translating percent to dB is straightforward. For example, the following steps translate THD + N% to THD + N dB, but the same steps can be used to translate SNR + D or SINAD from percent to dB.

$$\frac{\text{THD} + \text{N}\%}{100} = \text{THD} + \text{N} \tag{16}$$

Then:

$$20 \log (\text{THD} + \text{N}) = (\text{THD} + \text{N}) \text{ dB} \tag{17}$$

This can be put into one mathematical expression,

$$20\log_{10}\left(\frac{\text{THD} + \text{N}\%}{100}\right) = (\text{THD} + \text{N})\text{dB} \tag{18}$$

but it is often useful to have the intermediate step of a scalar number, because equation (16) is also stated in scalar numbers. To use this equation in dB, remember:

$\log B^{A} = A \times \log B$ and thus, equation (14) in dB is :

$$\text{SINAD dB} = \text{SNR} + \text{D dB} = (\text{THD} + \text{N dB})^{-1} = -(\text{THD} + \text{N}) \text{ dB} \tag{19}$$

The ability to convert between percent and dB simplifies matching the appropriate SINAD specifications between an amplifier and an ADC. Ideally, choosing an amplifier and an ADC that have the same SINAD realizes the full potential of the signal chain. In practice, choosing an amplifier that has a slightly higher SINAD ensures that it does not degrade the system performance.

For example, the TLV1572 ADC has a typical SNR+D of 58 dB that equates to an ENOB of 9.35 bits. An amplifier like the TLV2770 is an excellent choice to drive this ADC. The TLV2770 has more than sufficient GBP (5.1 MHz typical) to place significant gain on the input signal. Also, the THD+N graphs in the back of the TLV2770 data sheet match the performance of the TLV1572 in nearly all cases, with the only exception being a relatively high supply voltage and high signal gain.

5.7 ADC Bits

An ADC specification that varies with V_{CC} levels is the size of one least significant bit (LSB). This becomes clear with the following equation:

$$1\,\mathrm{LSB} = \frac{\mathrm{Vfullscale}}{2^{N} - 1} \tag{20}$$

Where n = resolution of the ADC

For the case of a 12-bit (ENOB) ADC, moving from a 5-V to 3-V full-scale range results in a reduction in size of 1 LSB from 1.22 mV to 732 μV. For an ADC like the TLV1572 with a V_{CC} range of 2.7 to 5.5 V, this results in a range of LSB size (5.37 mV to 2.64 mV). The main concern is that, particularly in moving a system to a lower voltage, the LSB does not shrink to the point of being susceptible to system parasitics.

The ADC is not a perfect component. There are errors that affect its accuracy. These errors affect the least significant bits and act as a limitation to ultimate system accuracy.

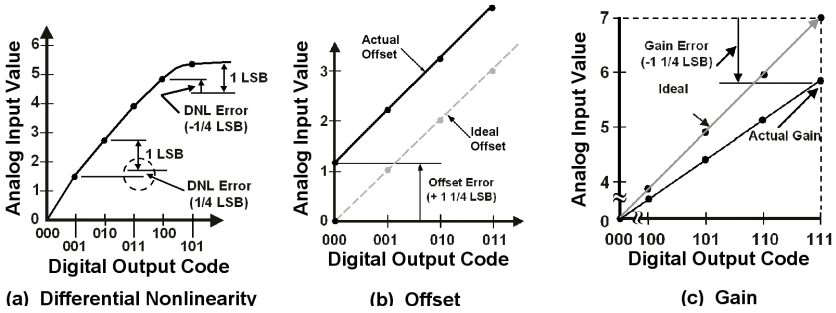

Figure 13. ADC Error Sources

These errors are of three different types:

- Differential nonlinearity, where the input voltage step size is not the same for each change in output code. It is shown in Figure 13(a).
- Offset error, where all of the input voltages have to be a fixed value above or below the ideal to produce changes in output code. It is shown in Figure 13(b).
- Gain error, which means that the change in voltage to produce digital codes is below or above the ideal gain / output code function. It is a cumulative error, shown in Figure 13(c).

These error sources are usually combined in the ADC data sheet and expressed as their sum. This specification is known as the *integral nonlinearity* (INL) of the ADC. It is the responsibility of the designer to understand these error sources and their implications. Ideally, a data converter would have zero bits of INL. In practice, however, the INL can be as large as ½ bit before the data converter has to be downgraded in ENOB. INL larger than ½ bit can be tolerated only if the source of the error is offset in an ac-coupled system. The designer may be forced to specify an ADC with more bits than originally thought, so that *throwing away* least significant bits can eliminate the INL error.

As conversion frequency increases, the ENOB will decrease. The reason is obvious—the conversion needs to be done with less and less settling time, and therefore more unpredictability in the value of input voltage.

5.8 ADC Input

Figure 14 shows an example of an op amp driving the input of an ADC. Designers probably recognize that the input of an ADC is a one-pole low pass filter. High-speed data converters can have a broad range of R_{ADC} from 500 Ω to 1 MΩ and an input capacitance of 1 to 5 pF. These, in large measure, determine the bandwidth of the part. Figure 14 does not necessarily imply that this capacitance is isolated—it may be distributed with R_{ADC} and therefore appears at the output of the buffer op amp. Unfortunately, even a small value of capacitance can cause instability in the buffer op amp stage, requiring isolation and compensation.

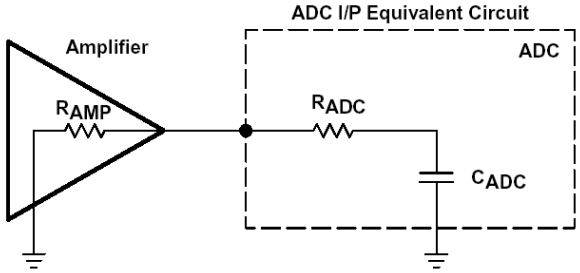

Figure 14. Amplifier–ADC Interface

Many high performance ADCs have differential inputs. In these cases, the input characteristics for each input are similar to the characteristics of a single-ended input.

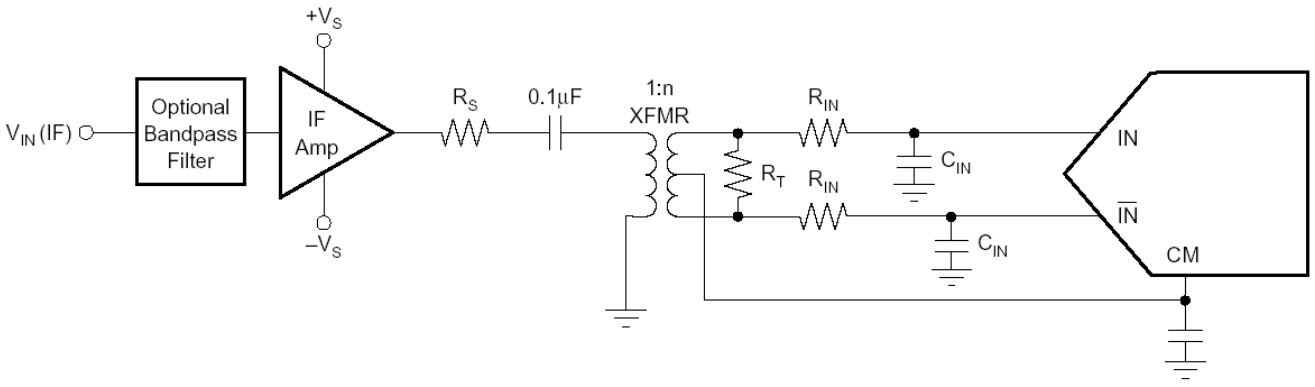

Figure 15. Example Base Station Application

A fully differential op amp may be substituted for the transformer-coupled approach above:

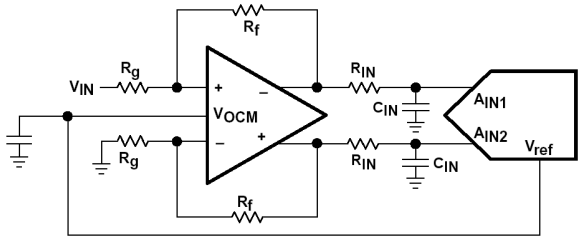

Figure 16. Fully Differential Input to the ADC

There are several features of the fully differential interface above that are important:

- This example shows that an input voltage V_{IN} is single ended, and is converted to a differential output by the fully differential op amp.
- The common mode operating point of the fully differential op amp (V_{OCM}) is set by the V_{ref} output of the ADC. The designer needs to be very careful not to overload the V_{ref} output of the data converter, as it may not be designed to drive much of a load. In the example above, it is also bypassed by a capacitor. A data converter may have a V_{ref+} and V_{ref-} output, which can be converted to single ended by an op amp buffer.
- There is a low pass filter network consisting of R_{IN} and C_{IN} on each input. The values are selected to form a single-pole low pass filter that eliminates high frequency interference without affecting the amplitude of the bandwidth of interest. Because a single-pole filter significantly rolls off amplitude before the –3 dB point, the –3 dB point is shifted to 2 to 5 five times the sample frequency. In this way, amplitude rolloff in the bandwidth of interest is negligible. R_{IN} also serves to isolate the op amp output from a capacitive load that would otherwise destabilize it. R_{IN} is usually selected to terminate the ADC input at 50 Ω, splitting the termination value between the two resistors.

5.9 Drive Current

Drive current from the amplifier is another consideration in driving the analog input of an ADC. The normal input resistance of an ADC can vary greatly, from 500 Ω to over 1 MΩ. RF designers are used to dealing with RF levels in dBm, and the input power required for a data converter with 500 Ω input resistance is in the range of 1 dBm. If the designer is not expecting it, the ADC can load an op amp output when the RC low pass filter discussed above has been added. Simply speaking, the series resistor on the op amp output forms a voltage divider with the ADC input. The designer is faced with losing accuracy due to the tolerance of the series resistor and the uncertainty of the absolute value of the input resistance of the ADC.

There are two ways of dealing with this problem. One is to delete the RC low pass filter completely, and live with potential high frequency interference and the input capacitance of the ADC, which could cause op amp instability and is obviously undesirable.

The other is to use auto calibration techniques to compensate for these tolerances, *throwing away* a few bits of conversion on the high and low end of the ADC conversion range. This assumes that the input signal is ac-coupled, and dc accuracy is not important.

5.10 Slew Rate - Revisited

When dealing with the ADC input itself, and the ADC used with a compensating low pass filter, there are rise time issues associated with the RC time constants involved. These show up as slew rate limitations, as discussed in the slew rate above. This discussion, however, describes the components external to the op amp that affect slew rate – the compensating low pass filter, and the ADC input. The capacitors affect the slew rate because the driving voltage must charge them.

This charge time is governed by the equation:

$$V(t) = V_O e^{-(t/RC)} \tag{21}$$

Where:

V_o is the steady state V on the capacitor.

Assuming the input voltage at the voltage source (V_s) is steady from t = – ∞ up until t = 0, it can be determined that $V_o = V_s$. The simple explanation is that, in a dc steady state, the capacitor acts like an open circuit, thus having the same voltage as V_s.

To further simplify the analysis, assume that V_s switches from a known voltage to ground. Solve the dual voltage divider equations to created a simple RC circuit.

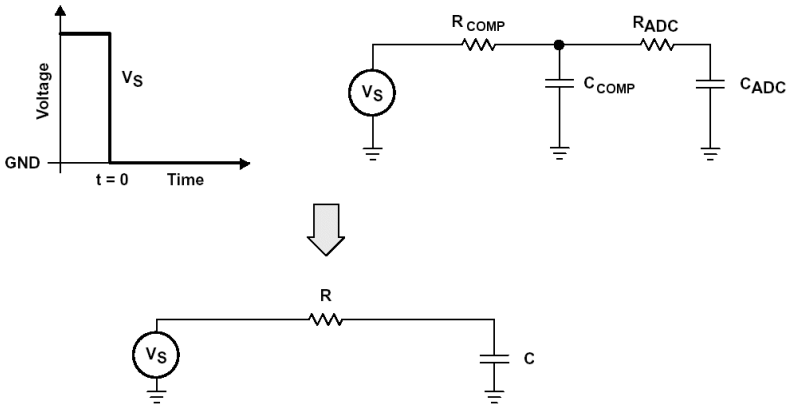

Figure 17. Circuit Simplification

It is intuitive that where t = 0, or right at the switch in potential, the current is the greatest while the voltage exponentially decays over time. The largest current the amplifier needs to handle can then be calculated roughly as:

$$I = \frac{V(t)}{R} \quad \text{Where } t = 0. \tag{22}$$

For example, using the TLV1544 ADC with no input RC network gives approximate values of R = 1 kΩ and C = 55 pF. The time constant τ can then be calculated, given the input resistance on the ADC. If the largest input voltage to the TLV1544 is 3 V, the amplifier needs to source roughly 3 mA.

5.11 Settling Time

When the input resistance is high, the input capacitance of the ADC predominates the load characteristics. The low pass filter described above becomes mandatory to isolate the output of the op amp from the input capacitance of the ADC. The capacitive load creates overshoot on the op amp output, creating settling time problems at the ADC input.

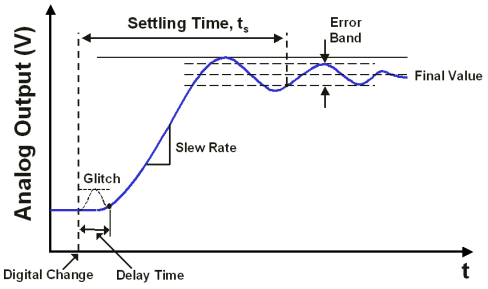

Figure 18. Settling Time Limitation

Figure 18 shows the complex nature of the op amp / ADC interface. Several features deserve notice:

- The voltage level can glitch due to the action of the output stages of the ADC. Proper decoupling techniques can reduce this effect.
- The slew rate of the overall interface affects how soon the analog voltage can be sampled.
- The action of the capacitors, causing a degree of ringing, will create an error band. The ringing will have a decay constant, causing the voltage to settle.

Only after waiting until the glitch is damped out, the slew rate analog voltage has changed, and the transitions have settled can a new sample be taken.

5.12 Signal Bias

Using the proper signal bias to the input waveform is another important consideration regarding the analog input of the ADC. Different ADCs have different analog input ranges.

For example, the TLV1572 has a single-ended analog input with a voltage range that extends 0.3 V beyond each rail. Conversely, the TLV1562 allows single-ended inputs similar to the TLV1572, and differential inputs (approximately 2 Vpp) operated in a different mode. Furthermore, some converters like the TLC320AD50 use a completely differential input structure. Understanding what the analog input voltage range looks like allows the designer to properly gain and bias an input signal and take advantage of the full dynamic range of the ADC.

Many circuits exist that properly bias an analog input signal. Two proven circuits for this function per the 1998 TI Analog Seminar are included below. Both circuits bias an ac input signal at mid-rail on a single supply amplifier.

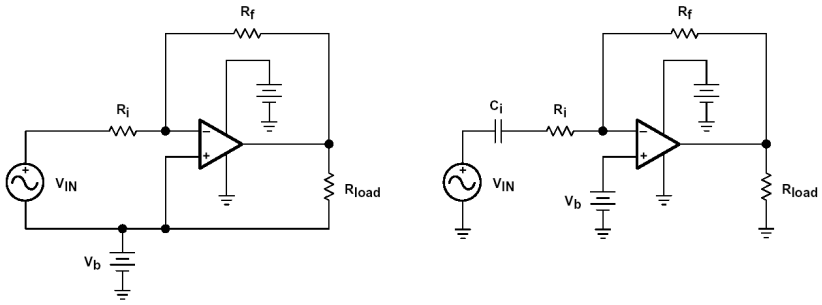

Figure 19. Input Signal Biasing Circuits

Obviously, the solution on the left hand side of Figure 19 is unacceptable, because it is probably impossible to reference both the source and the load to a potential other than ground. In the right hand side figure, the potential V_b is isolated from V_{IN} by coupling capacitor C_i, but appears on the load R_{load}.

5.13 Input Offsets

Input offset voltage (V_{IO}) is another parameter to consider on the amplifier. Even in a simple biasing or buffering application the amplifier introduces a dc error induced by the voltage difference inherent to the amplifier inputs and denoted in the data sheet by V_{IO}.

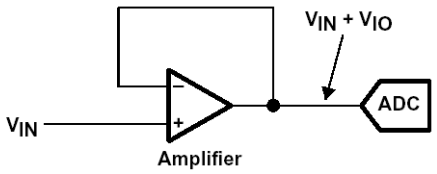

Figure 20. Input Offset Voltage (V_{IO})

The other important input error on the amplifier is input bias current, I_{IB}, which can be a very significant error if a relatively small current represents the signal on which the amplifier is working. As an example, some types of sensors can fall into this category. While V_{IO} is often easier to visualize, input current errors can also drastically affect resolution errors in an application. In general, it is good practice to keep the combination of both of these errors below 0.5 LSB in size, referenced to the size of one LSB on the data converter.

6 Power Supply

Of course, devices used in the design must be able to withstand and function with the voltages used on a board. While this is obvious, there are other less obvious points that need to be explored, including power and ground planes, input/output voltage range, and the size of 1 LSB on the ADC.

6.1 Power and Ground Planes

Ideally, a board has both an analog and a digital ground plane. This helps isolate sensitive analog circuits—like an amplifier—from switching noise associated with the digital circuits. If a separate analog supply and ground plane are not possible, the power supply rejection ratio (PSRR) specification identifies problems that may be encountered from power supply noise. For newer amplifiers like the TLV2450, there is often a PSRR vs frequency graph in the back of the data sheet that can help if a designer understands the frequency characteristics of noise being encountered on the power rail.

6.2 Input/Output Voltage Range

Another effect of choosing any V_{CC} can be the input and output voltage range on the amplifier. Up until relatively recently, most amplifiers did not supply inputs and outputs that could swing to both rails. For example, the TLC2272 provides rail-to-rail outputs (RRO) but not rail-to-rail inputs (RRI). Instead, the TLC2272 has 1.5 V of headroom on the upper rail of the input. Thus, on a 10-V supply, the TLC2272 has an input range from GND to 8.5 V. Similarly, for a V_{CC} of 5 V, the TLC2272 still has 1.5 V of headroom and an input range from GND to 3.5 V.

The evolution of the amplifier has led to the innovation of rail-to-rail input and output (RRIO) amplifiers such as the TLV2462. RRIO amplifiers allow signals to swing between both rails, thus eliminating headroom on the inputs or outputs. This becomes increasingly important in low voltage applications, as a designer has a smaller input/output range with which to work. RRI comes at a price, however. Today, the construction of a rail-to-rail input stage introduces crossover distortion. For distortion-sensitive applications, the designer should consult both the op-amp vendor and the data sheet to determine the suitability of a particular amplifier.

7 Summary

This report briefly covered various issues to consider when interfacing an op amp to an ADC. With these things in mind, it should be straightforward to sift through many amplifier choices and find parts that interface nicely to an ADC and optimize system performance.

Summary Checklist

- Bandwidth – amplifier GBP vs ADC speed
- Resolution – amplifier SINAD vs ADC ENOB
- Analog Input – τ, drive current, and input signal vs ADC analog input range
- Power – amplifier PSRR, amplifier I/O voltage range, and ADC LSB

8 References

1. *Electric Circuit Analysis Second Edition*, by Johnson, Johnson, and Hilburn Copyright 1992, Prentice Hall, Englewood Cliffs NJ
2. *DSP/Analog Technologies 1998 Seminar Series*, by Texas Instruments Incorporated Copyright 1998
3. *Op Amps for Everyone,* Ron Mancini, Editor, Texas Instruments SLOD006, Copyright 2000
4. *Intuitive Operational Amplifier,* Thomas M. Frederickson, Mc Graw Hill, Copyright 1988

Appendix A: Design Example – Cellular Telephone Base Station

ADC Considerations

Any discussion of the performance of a cellular base station design must center on the performance of the data converter used to digitize the intermediate frequency (IF) bandwidth. The proper selection of data converter determines, to a large degree, the RF performance of the base station. Therefore, the choice of data converter is usually made long before the designer begins the design of an op amp interface. The designer must make certain that the op amp interface does not act as a limiting function in overall system performance.

The dc nonlinearity performance is not nearly as important in a communications ADC as it is in an instrumentation ADC because signals are band limited. The dynamic performance of the ADC is critical in communications applications. The overall receiver system specifications depend heavily on ADC dynamic performance. Characteristics of the data converter include:

- Effective number of bits (ENOB) - is usually measured and specified at the system operating frequency, so it is a real performance measurement.
- Spurious Free dynamic range (SFDR) – determines the ADC's ability to separate an incoming signal from ADC noise spikes.
- Total Harmonic Distortion (THD) – is a measure of the distortion that the ADC adds to the signal.
- Signal-to-noise ratio (SNR) – includes ADC noise and noise from other sources.
- Sampling Rate
- Full scale range (FSR)

ADC Requirements for Processing GSM Signal

The data converter requirements for a cellular base station also depend on the communications protocol selected. The two most common are CDMA and GSM. This example focuses on GSM. It is beyond the scope of this document to examine the details of the GSM specification, but some of the high points are:

- $SNR_{THERMAL}$= 9 dB for GSM-900
- Process gain required = 24 dB (fS/BW)
- Selected ADC_{SNR} = 37 dB better than thermal
- Baseband converter = 46 dB SNR
- SNR_{ADC} = (46-24) = 22 dB
- ENOB (effective number of bits) = (SNR-1.76) / 6.02 = 3.36 bits signal (4 bits required)
- Interferer = 40 dB ≈ 6.3 bits

The mean squared quantization power is $P_{qn} = q_s^2 / 12R$, where q_s is the quantization step size and R is the ADC input resistance, typically 600 Ω to 1000 Ω. Communication ADCs similar to the THS1052 and THS1265 typically have a full-scale range (FSR) of 1 Vpp to 2 Vpp. Based on the assumption of a 50 Ω input/output termination, the quantization noise power for a 12 bit, 65 MSPS ADC is –74 dBm. The receiver noise power in a noise-limited receiver can be computed as the thermal noise power in the given receiver BW plus the receiver noise figure.

For a 200 kHz BW GSM channel, T_A = 25 °C, and 4 to 6 dB NF, the receiver noise power is -115 dBm. To boost the receiver noise to the quantization noise power level requires a gain of 42 dB. The smallest 1% bit error-rate (BER) for GSM-900 is –104 dBm, thus the SNR at baseband due to the thermal noise component is given by $SNR_{THERMAL} = E_b/N_o$ = -104 dBm +115 dBm = 9 dBm. For a raw BER to be 1% in a GSM system, testing and standard curves indicate that a baseband SNR of 9 dB is needed for this performance.

The process gain is $G_p = f_s / BW = 52 \times 10^6 / 200 \times 10^3 = 2.6 \times 10^2$ = 24 dB where the GSM channel BW is 200 kHz and f_s is 52 MHz (ADC sampling frequency). The converter noise at baseband should be much better than the radio noise (thermal noise plus process gain), hence the converter noise at baseband = SNR_{ADC} + process gain (G_p).

SNR_{ADC} is selected as 37 dB better than $SNR_{THERMAL}$; baseband converter noise is 9 dB + 37 dB = 45 dB. SNR_{ADC} required to meet the GSM-900 standard is (46-24) dB = 22 dB. The ENOB of the ADC must be = (SNR-1.76) / 6.02 @ 4 bits. Assuming that the filter attenuates the interferer by 50 dB, the interferer drops from 113 dBm to -53 dBm, or 40 dB above the GSM signal. The number of bits required to accommodate the interferer is 40 dB / 6 dB / bit = 6.3 bits. Six bits are required to accommodate the interferer, 4 bits are required for the GSM signal, and 2 bits are required for headroom, so we need a 12-bit converter.

Table 3. Op Amp Requirements

Parameter	Value	OPA685	Units
Noise voltage	2.7 to 8	2.7	$nV/\sqrt{Hz}$
Noise current	1 to 30	11.9	$pA/\sqrt{Hz}$
THD	70 to 95	82	dBc
Slew Rate	260 to 3500	1700	V/µS
Small signal bandwidth	200 to 600	900	MHz
Large signal bandwidth	≥100	135	MHz
Common-mode input voltage	3	±2.9	V
Supply voltage	±5	±5V	V
Settling time	8 to 20	15	nS
Output current	40 to 100	80	mA
Output impedance	≤ 20	0.02	Ω
PSRR	-60	-64	dB
CMRR	-70	50	dB
Input offset voltage	10	± 5	mV

The SFDR and IMD are the key ADC/DAC parameters that influence op amp selection. A minimum requirement is that the op amp's SFDR or IMD, measured at the operating frequency, is 5 dB to 10 dB better than the converter's equivalent specifications. A perfect 12-bit ADC has a SFDR or IMD of 72 dB, and the op amp should have a SFDR or IMD of 77 dB to 82 dB. Fast settling time is mandatory because the ADC must settle within a fraction of an LSB in the ADC sampling time.

Low voltage systems are popular now, and the designer must be aware that ac specifications are only valid at the test supply voltage. Operating the op amp at different supply voltages changes their ac specifications.

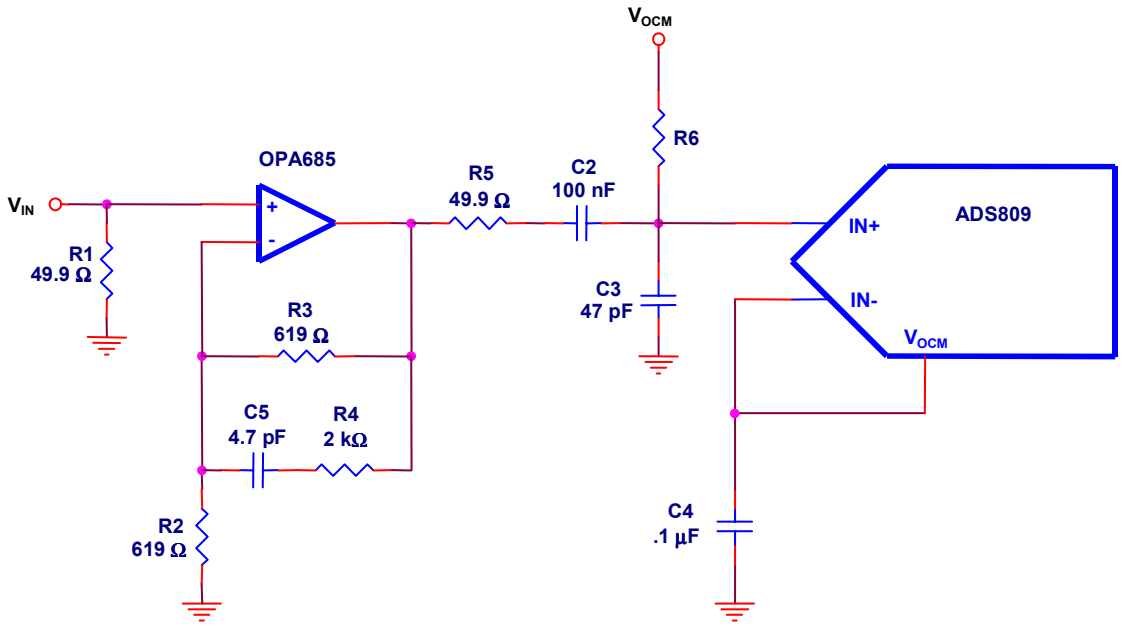

Figure 21. Example of Buffer Op Amp Design

This is an example of an ADC buffer op amp design. The input is terminated with R1, a 49.9-Ω resistor. The OPA685 is a current feedback amplifier, operated at a noninverting gain of 2 (as set by R3 and R2). C5 and R4 are compensation components (never put a capacitor directly across the feedback of a current feedback amplifier). The 49.9-Ω resistor in series with the amplifier output (R5), in combination with the 47 pF capacitor to ground (C3), are compensation for the input capacitance of the ADC converter. R5 also isolates the output of the amplifier from a capacitive load. C2 ac-couples the amplifier output, and R6 to V_{OCM} biases the input voltage up to the common mode range of the converter. Its value is not critical.

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